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SUGHRUE MION ZINN MACPEAK & SEAS
2100 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20037-3213

EXAMINER

RYMAN, DANIEL J

ART UNIT	PAPER NUMBER
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2665

9

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/462,895

Applicant(s)

CHITRE ET AL.

Examiner

Daniel J. Ryman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 14 and 18 is/are allowed.
- 6) ☒ Claim(s) 1-13, 15-17 and 19-38 is/are rejected.
- 7) ☒ Claim(s) 39 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Amendment A, filed 11/5/2003, with respect to the rejection(s) of claim(s) 1-39 under Iidaka et al (USPN 5,528,590); Easki et al (USPN 5,440,547); Yamashita (USPN 5,341,376); Jurkevich et al (USPN 5,282,207); Chitre et al (USPN 5,600,653); Nakagaki et al (USPN 5,657,316); and Shobatake et al (USPN 5,557,609) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Nishimura (USPN 5,570,362); Woo et al (USPN 5,425,101); Carr (USPN 5,293,379); and Scarpa (USPN 5,444,743).

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because the abstract does not avoid "the form and legal phraseology often used in patent claims, such as "means" and "said."" Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-5, 8, 13, 19-23, 25, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (USPN 5,570,362).

6. Regarding claims 1, 19, and 21, Nishimura discloses a method for encoding ATM cells comprising the steps of: receiving an information stream (col. 5, lines 6-22); assembling a header frame (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), where, as broadly defined, the header is a frame since the header is the minimum unit of transfer; assembling a payload frame (col. 5, lines 6-54 and col. 6, line 32-col. 7, line 49); and placing idle/unassigned cells in a selected portion of the payload frame (col. 6, line 46-col. 7, line 9). Nishimura does not expressly disclose receiving an ATM cell stream comprised of a plurality of ATM cells; detecting idle/unassigned cells within said cell stream; assembling a header frame made up of headers of a number of said plurality of ATM cells; assembling a payload frame made up of pay-loads of said number of said plurality of ATM cells; and placing some of the detected idle/unassigned cells in a selected portion of the payload frame; however, Nishimura additionally discloses that, where a typical ATM cell stream wastes bandwidth due to overhead, Nishimura's ATM cell stream is more bandwidth efficient. Examiner takes official notice that protocol conversions are well known in the art. Thus Nishimura suggests receiving an ATM cell stream comprised of a plurality of ATM cells, where the ATM cell stream uses bandwidth inefficiently; detecting

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idle/unassigned cells within said cell stream in order to remove the idle/unassigned cells to increase bandwidth efficiency; assembling a header frame made up of headers of a number of said plurality of ATM cells, where Nishimura's header contains information similar to an ATM header (col. 5, lines 29-36) such that the VPI/VCI information of the cells in the cell stream is preserved; assembling a payload frame made up of pay-loads of said number of said plurality of ATM cells; and placing some of the detected idle/unassigned cells in a selected portion of the payload frame in order to have a cell of the correct length. It would have been obvious to one of ordinary skill in the art at the time of the invention to receive an ATM cell stream comprised of a plurality of ATM cells; detect idle/unassigned cells within said cell stream; assemble a header frame made up of headers of a number of said plurality of ATM cells; assemble a payload frame made up of pay-loads of said number of said plurality of ATM cells; and place some of the detected idle/unassigned cells in a selected portion of the payload frame in order to increase the efficiency of bandwidth use in an ATM cell stream.

7. Regarding claim 2, referring to claim 1, Nishimura discloses that the header frame is arranged in an i row \times n column matrix (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), where, as broadly defined, the header can be viewed as containing one row and n columns where each column contains an octet or a bit of information (e.g. a value in a 1×4 matrix would be ABCD).

8. Regarding claims 3 and 22, referring to claims 1 and 21, Nishimura discloses that the payload frame is arranged in an j row \times m column matrix (col. 5, lines 6-54 and col. 6, line 32-col. 7, line 49), where, as broadly defined, the payload can be viewed as containing one row and

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m columns where each column contains an octet of information (e.g. a value in a 1x4 matrix would be ABCD).

9. Regarding claim 4, referring to claim 1, Nishimura discloses that the step of assembling said header frame further comprises: partitioning said header frame comprised of headers of an n number of ATM cells into a first section and a second section; said first section comprised of n - x number of headers of said n number of ATM cells and an added cell made up of control bytes; and said second section comprised of x number of headers of said n number of ATM cells (col. 5, lines 29-36) where “x” could be 0 and where “comprising” is a broad phrase which only requires one set of header information as long as the header information is the same for all of the cells in the frame (i.e. the header contains the VP and VC information for all of the cells in the frame where all the cells have the same VP and VC information).

10. Regarding claim 5, referring to claim 1, Nishimura discloses that the step of assembling said header frame further comprises: adding a predetermined number of bytes of Header Error Correction Code (HEC) to said header frame (col. 6, lines 6-17 and col. 10, lines 24-39).

11. Regarding claim 8, referring to claim 1, Nishimura discloses that the step of assembling said payload frame further comprises: adding a predetermined number of bytes of Payload Error Correction Code (PECC) to said payload frame (col. 9, lines 29-43).

12. Regarding claims 13 and 25, Nishimura discloses receiving an information stream (col. 5, lines 6-22); assembling a header frame (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), where, as broadly defined, the header is a frame since the header is the minimum unit of transfer; assembling a payload frame (col. 5, lines 6-54 and col. 6, line 32-col. 7, line 49); adding Payload Error Correction Code to the payload (col. 9, lines 29-43); placing idle/unassigned cells

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in a selected portion of the payload frame (col. 6, line 46-col. 7, line 9); and storing a count of the number of idle/unassigned cells contained in the payload frame in a second control byte within a trailer frame (col. 6, line 62-col. 7, line 9). Nishimura does not expressly disclose detecting idle/unassigned cells within said cell stream, assembling an ATM frame having a header frame made up of headers of a first predetermined number of said plurality of ATM cells and a payload frame made up of payloads of said first predetermined number of said plurality of ATM cells, placing up to a second predetermined number of the detected idle/unassigned cells in a selected portion of the payload frame, and adding Payload Error Correction Code to those idle/unassigned cells which are placed in said selected portion of said payload frame; and storing an idle/unassigned cell indicator in a first control byte in said header frame to be transmitted over said wireless link which indicates whether or not idle/unassigned cells have been placed at said selected portion of said payload frame; and storing a count of the number of idle/unassigned cells contained in the payload frame in a second control byte within said header frame; however, Nishimura additionally discloses that, where a typical ATM cell stream wastes bandwidth due to overhead, Nishimura's ATM cell stream is more bandwidth efficient. Examiner takes official notice that protocol conversions are well known in the art. Thus, Nishimura suggests receiving an ATM cell stream comprised of a plurality of ATM cells, where the ATM cell stream uses bandwidth inefficiently, detecting idle/unassigned cells within said cell stream in order to remove the idle/unassigned cells to increase bandwidth efficiency, assembling an ATM frame having a header frame made up of headers of a first predetermined number of said plurality of ATM cells, where Nishimura's header contains information similar to an ATM header (col. 5, lines 29-36) such that the VPI/VCI information of the cell stream is preserved, and a payload

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frame made up of payloads of said first predetermined number of said plurality of ATM cells, placing up to a second predetermined number of the detected idle/unassigned cells in a selected portion of the payload frame in order to have a cell of the correct length, and adding Payload Error Correction Code to those idle/unassigned cells which are placed in said selected portion of said payload frame in order to ensure proper delivery of the frame; and storing an idle/unassigned cell indicator in a first control byte in said header frame to be transmitted over a link which indicates whether or not idle/unassigned cells have been placed at said selected portion of said payload frame; and storing a count of the number of idle/unassigned cells contained in the payload frame in a second control byte within said header frame where storing control information in a header is equivalent to storing the information in a trailer. It would have been obvious to one of ordinary skill in the art at the time of the invention to detect idle/unassigned cells within said cell stream, assemble an ATM frame having a header frame made up of headers of a first predetermined number of said plurality of ATM cells and a payload frame made up of payloads of said first predetermined number of said plurality of ATM cells, place up to a second predetermined number of the detected idle/unassigned cells in a selected portion of the payload frame, and add Payload Error Correction Code to those idle/unassigned cells which are placed in said selected portion of said payload frame; and store an idle/unassigned cell indicator in a first control byte in said header frame to be transmitted over a link which indicates whether or not idle/unassigned cells have been placed at said selected portion of said payload frame; and store a count of the number of idle/unassigned cells contained in the payload frame in a second control byte within said header frame in order to increase the efficiency of bandwidth use in an ATM cell stream. Nishimura does not expressly disclose that

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the link is a wireless link; however, Nishimura does disclose that the variable length ATM cells use bandwidth more efficiently than normal ATM cells (col. 4, lines 19-51). Examiner takes official notice that it is well known in the art that bandwidth efficiency is important on wireless links. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use this invention on a wireless link, where a stream of normal ATM cells is received over a wire link and the variable length ATM cells are transmitted over the wireless link.

13. Regarding claim 20, referring to claim 19, Nishimura discloses that the step of assembling said header frame further comprises: partitioning said header frame comprised of headers of said predetermined number of ATM cells into a first section and a second section; said first section comprised of a second predetermined number of headers from said first predetermined number of ATM cells and an added cell made up of control bytes; and said second section comprised of having a third predetermined number of headers from said first predetermined number of ATM cells (col. 5, lines 29-36) where “predetermined number” is a broad phrase which includes the number 0.

14. Regarding claim 23, referring to claim 22, Nishimura discloses that the step of assembling said payload frame further comprises: adding a predetermined number of bytes of Payload Error Correction Code (PECC) to all i number of rows of said payload frame (col. 9, lines 31-47) where i is 20 (add to every other 6-octet units).

15. Regarding claim 31, incorporating arguments from the rejection of claims 1-3 and 13, Nishimura suggests an apparatus for receiving an ATM cell stream sequence via a wireless link (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), encoding said ATM cell stream

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for transmission of data via a wireless link (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), receiving and decoding encoded wireless data received via said wireless link and transmitting another ATM cell stream sequence via said wireline link (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), comprising: a wireline interface for receiving said cell stream sequence from said wireline link and transmitting said another cell stream sequence (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49); an encoder receiving cell stream data from said wireline interface, encoding said cell stream data and outputting encoded cell data (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49); a wireless interface for receiving said encoded cell data from said encoder, transmitting said encoded cell data via said wireless link and receiving previously encoded cell data (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49); a decoder receiving said previously encoded cell data from said wireless interface, decoding said previously encoded cell said data and outputting said another cell stream sequence to said wireline interface; and a control unit for controlling said interfaces, encoder and decoder (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49).

16. Claims 6, 9, 24, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (USPN 5,570,362) as applied to claims 5, 8, and 23 above, and further in view of Matsushita (USPN 5,608,738).

17. Regarding claim 6, referring to claim 5, Nishimura does not expressly disclose that the Header Error Correction Code is generated using a Reed-Solomon coding scheme. Matsushita teaches, in a packet communication system, using a Reed-Solomon coding scheme to generate correction code since Reed-Solomon is a well-known error correction code (col. 4, line 45-col. 5, line 62). It would have been obvious to one of ordinary skill in the art at the time of the invention

to use a Reed-Solomon coding scheme to generate correction code since Reed-Solomon is a well-known error correction code.

18. Regarding claims 9 and 24, referring to claims 8 and 23, Nishimura does not expressly disclose that the Payload Error Correction Code is generated by a Reed-Solomon coding scheme. Matsushita teaches, in a packet communication system, using a Reed-Solomon coding scheme to generate correction code since Reed-Solomon is a well-known error correction code (col. 4, line 45-col. 5, line 62). It would have been obvious to one of ordinary skill in the art at the time of the invention to use a Reed-Solomon coding scheme to generate correction code since Reed-Solomon is a well-known error correction code.

19. Regarding claim 27, referring to claim 25, Nishimura does not expressly disclose generating a header syndrome; and identifying bits in error using said header syndrome; wherein when a single bit in error is identified in the header, correction of said bit in error is performed, and when multiple bits in error are identified in the header, an ATM cell containing said multiple bits in error is dropped and replaced by an idle/unassigned cell. Matsushita teaches, in a packet communication system, using a Reed-Solomon coding scheme (header syndrome) to generate correction code since Reed-Solomon is a well-known error correction code (col. 4, line 45-col. 5, line 62). It would have been obvious to one of ordinary skill in the art at the time of the invention to generate a header syndrome (Reed-Solomon) and identify bits in error using said header syndrome wherein when a single bit in error is identified in the header, correction of said bit in error is performed in order to correct bit errors. Nishimura in view of Matsushita does not expressly disclose that an ATM cell containing said multiple bits in error is dropped and replaced by an idle/unassigned cell; however, Examiner takes official notice that this is well known in the

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art. It would have been obvious to one of ordinary skill in the art at the time of the invention to drop a cell that cannot be corrected as is well known in the art.

20. Claims 7, 26, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (USPN 5,570,362) as applied to claims 1 and 25 above, and further in view of Naimpally et al (USPN 5,650,825).

21. Regarding claims 7 and 26, referring to claims 1 and 25, Nishimura does not expressly disclose that the step of placing idle/unassigned cells further comprises: adding extra Payload Error Correction Code in any idle/unassigned cells which are placed in said selected portion of said payload frame; however, Nishimura does disclose adding Payload Correction Code to a payload frame (col. 9, lines 29-43). Naimpally teaches using idle/unassigned cells to transport additional information in order to take advantage of otherwise wasted bandwidth (col. 4, lines 15-40; col. 4, line 66-col. 5, line 5; and col. 12, lines 1-7). It would have been obvious to one of ordinary skill in the art at the time of the invention to add extra Payload Error Correction Code in any idle/unassigned cells which are placed in said selected portion of said payload frame in order to take advantage of otherwise wasted bandwidth by increasing the level of error correction in the system.

22. Regarding claim 28, incorporating arguments from claim 1, Nishimura does not expressly disclose inserting error correction code into some of said idle/unassigned cells; setting a first information field within said frame at a first state when error correction code has been inserted into any idle/unassigned cells within said frame; and setting said first information field at a second state when no error correction code has been inserted into idle/unassigned cells within said frame; however, Nishimura does disclose adding Payload Correction Code to a payload

frame (col. 9, lines 29-43). Naimpally teaches using idle/unassigned packets to transport additional information in order to take advantage of otherwise wasted bandwidth (col. 4, lines 15-40; col. 4, line 66-col. 5, line 5; and col. 12, lines 1-7). Naimpally also teaches including an indication of whether or not information has been included in the idle/unassigned packets (col. 4, lines 52-65) where it is implicit that this is done in order to ensure that the data is properly received. It would have been obvious to one of ordinary skill in the art at the time of the invention to insert error correction code into some of said idle/unassigned cells; set a first information field within said frame at a first state when error correction code has been inserted into any idle/unassigned cells within said frame; and set said first information field at a second state when no error correction code has been inserted into idle/unassigned cells within said frame in order to take advantage of otherwise wasted bandwidth by increasing the level of error correction in the system.

23. Regarding claim 29, referring to claim 28, Nishimura in view of Naimpally suggests storing a number of idle/unassigned cells used for extra error correction code in a second information field within said frame when said first information field has been set at said first state (Nishimura: col. 6, line 62-col. 7, line 9 and Naimpally: col. 4, lines 15-40; col. 4, line 66-col. 5, line 5; and col. 12, lines 1-7). Nishimura teaches storing a number (length) of effective and ineffective data (Nishimura: col. 6, line 62-col. 7, line 9). Naimpally teaches storing an indicator which indicates if data is stored in idle frames (Naimpally: col. 4, lines 15-40; col. 4, line 66-col. 5, line 5; and col. 12, lines 1-7). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to store a number of idle/unassigned cells used for extra error correction code in a second information field within said frame when said first

information field has been set at said first state in order to allow the receiver to determine what is effective and ineffective data.

24. Claims 10-12, 17, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (USPN 5,570,362) in view of Woo et al (USPN 5,425,101).

25. Regarding claim 10, incorporating arguments from the rejection of claims 1-3 and 13, Nishimura discloses a method for transmitting ATM cells received from a wireline interface over a wireless link comprising: receiving an ATM cell stream comprised of a plurality of ATM cells from said wireline interface (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49); encoding said plurality of ATM cells, wherein said encoding step includes the steps of: detecting idle/unassigned cells within said cell stream (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), assembling a header frame made up of headers of a first predetermined number of said plurality of ATM cells arranged in a first matrix (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), where, as broadly defined, the header is arranged in a matrix while it is in a buffer, assembling a pay-load frame made up of payloads of said first predetermined number of said plurality of ATM cells arranged in a second matrix (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49) where, as broadly defined, the header is arranged in a matrix while it is in a buffer, and placing up to a second predetermined number of the detected idle/unassigned cells to an end of the payload and header frames starting with a last column of each of said frames (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), where the predetermined number could be any number including zero and one. Nishimura does not disclose transmitting said predetermined number of said plurality of ATM cells over said wireless link by interleaving said header frame and said payload frame. Woo teaches, in a wireless system, interleaving frames

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together in order to reduce the impact of errors on the data stream (col. 9, lines 28-43). It would have been obvious to one of ordinary skill in the art at the time of the invention to transmit the predetermined number of the plurality of ATM cells over the wireless link by interleaving the header frame and the payload frame in order to reduce the impact of errors on the data stream.

26. Regarding claim 11, referring to claim 10, Nishimura in view of Woo suggests that the step of transmitting further comprising: interleaving by transmitting a third predetermined number of bytes from said payload frame for every byte transmitted from said header frame (Nishimura: col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49 and Woo: col. 9, lines 28-43) where the predetermined number could be any number.

27. Regarding claim 12, referring to claim 10, Nishimura in view of Woo disclose adding a synchronizing pattern to said header and payload frames (Nishimura: col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49 and Woo: col. 4, lines 50-57). Nishimura in view of Woo do not expressly disclose adding a two byte synchronization pattern. It is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1055); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Thus, since Nishimura in view of Woo disclose adding a synchronization pattern, it would have been

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obvious add any length of synchronization pattern, including two bytes, absent a showing of criticality by Applicant.

28. Regarding claim 17, referring to claim 15, Nishimura in view of Woo suggest generating a header syndrome (Reed-Solomon) (Woo: col. 4, lines 50-57 and col. 9, lines 28-43); and identifying bits in error using said header syndrome (Woo: col. 4, lines 50-57 and col. 9, lines 28-43); wherein when a single bit in error is identified in the header, correction of said bit in error is performed (Woo: col. 4, lines 50-57 and col. 9, lines 28-43). Nishimura in view of Woo do not expressly disclose that when multiple bits in error are identified in the header, an ATM containing said multiple bits in error is dropped and replaced by an idle/unassigned cell; however, Examiner takes official notice that this is well known in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to drop a cell that cannot be corrected as is well known in the art.

29. Regarding claim 32, referring to claim 31, Nishimura suggests that the encoder further comprises: a cell preprocessor for receiving said cell stream data (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), monitoring header bytes of incoming cells (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), detecting idle/unassigned cells and outputting cell data (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49); a frame assembler for receiving said cell data from said cell preprocessor (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49), assembling said data in a frame and outputting said frame (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49); an encoder unit for receiving said frame and encoding said frame according to a predetermined coding scheme (col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49). Nishimura does not disclose an interleaver for interleaving and

transmitting said frame to said wireless interface. Woo teaches, in a wireless system, interleaving frames together in order to reduce the impact of errors on the data stream (col. 9, lines 28-43). It would have been obvious to one of ordinary skill in the art at the time of the invention to have an interleaver for interleaving and transmitting said frame to said wireless interface in order to reduce the impact of errors on the data stream.

30. Regarding claim 33, referring to claim 31, Nishimura does not disclose that the decoder further comprises: an acquisition and synchronization unit for receiving previously encoded cell data from said wireless interface, searching for a predetermined synchronization pattern in said previously encoded cell data, declaring a synchronization pattern, and outputting interleaved cell data; a byte deinterleaver for deinterleaving said interleaved cell data received from said acquisition and synchronization unit, deinterleaving said interleaved cell data and outputting deinterleaved cell data; a decoder for decoding said deinterleaved cell data received from said byte deinterleaver according to a predetermined coding scheme and outputting decoded cell data; and a cell assembler for receiving said decoded cell data, assembling the decoded cell data into said another cell stream sequence, and outputting said another cell stream data to said wireline interface for transmission via said wireline link. Woo teaches, in a wireless system, interleaving frames together in order to reduce the impact of errors on the data stream (col. 9, lines 28-43). It would have been obvious to one of ordinary skill in the art at the time of the invention to have an interleaver for interleaving and transmitting said frame to said wireless interface in order to reduce the impact of errors on the data stream. Woo also teaches the use of a synchronization pattern in order to aid in synchronization (col. 4, lines 50-57). It would have been obvious to one of ordinary skill in the art at the time of the invention to use synchronization patterns in order to

achieve synchronization. Thus, Nishimura in view of Woo suggests the decoder further comprises: an acquisition and synchronization unit for receiving previously encoded cell data from said wireless interface, searching for a predetermined synchronization pattern in said previously encoded cell data, declaring a synchronization pattern, and outputting interleaved cell data (Woo: col. 4, lines 50-57 and col. 9, lines 28-43); a byte deinterleaver for deinterleaving said interleaved cell data received from said acquisition and synchronization unit, deinterleaving said interleaved cell data and outputting deinterleaved cell data (Woo: col. 4, lines 50-57 and col. 9, lines 28-43); a decoder for decoding said deinterleaved cell data received from said byte deinterleaver according to a predetermined coding scheme and outputting decoded cell data (Nishimura: col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49); and a cell assembler for receiving said decoded cell data, assembling the decoded cell data into said another cell stream sequence, and outputting said another cell stream data to said wireline interface for transmission via said wireline link (Nishimura: col. 4, line 46-col. 5, line 54 and col. 6, line 32-col. 7, line 49).

31. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carr (USPN 5,293,379) in view of Naimpally et al (USPN 5,650,825).

32. Regarding claim 15, Carr discloses a method of transmitting data over a link comprising the steps of: receiving a plurality of packets each having a header and a payload, said header including at least one field (length) (col. 5, line 46-col. 6, line 20); dropping said at least one field (length) from said header of each packet to thereby leave an unoccupied byte space in said header (col. 5, line 46-col. 6, line 20). Carr does not expressly disclose that a Header Error Correction (HEC) byte is dropped; however, Carr does disclose that Error Correction

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information (FCS) may be dropped from a frame (col. 5, line 46-col. 6, line 20). It would have been obvious to one of ordinary skill in the art at the time of the invention to drop the HEC since the HEC is "recalculatable" and thus the information can be derived at the receiver. Carr also does not disclose that the link is a wireless link or that the data is ATM cells; however, Examiner takes official notice that wireless links are well known in the art as well as ATM cells. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a wireless link and ATM cells. Additionally, Carr does not disclose inserting other non-HEC information into said unoccupied byte space; and transmitting each of said plurality of ATM cells. Naimpally teaches using idle/unassigned cells to transport additional information in order to take advantage of otherwise wasted bandwidth (col. 4, lines 15-40; col. 4, line 66-col. 5, line 5; and col. 12, lines 1-7). It would have been obvious to one of ordinary skill in the art at the time of the invention to insert other non-HEC information into the unoccupied byte space in order to take advantage of otherwise unoccupied bandwidth.

33. Regarding claim 16, referring to claim 15, Carr in view of Naimpally discloses regenerating said Header Error Correction byte from the remaining bytes in said header of each ATM cell after transmission of each cell (Carr: col. 5, line 46-col. 6, line 20).

34. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolf (USPN 5,892,770).

35. Regarding claim 30, Wolf discloses a method of restoring an ATM cell stream sequence comprising the steps of: recording the original positions of idle/unassigned cells in a cell stream sequence before being moved during assembly of an ATM frame prior to transmission of said frame over a link (col. 2, line 37-col. 3, line 13 and col. 6, lines 35-56) where, as broadly

defined, the positions are recorded since the structural data “are distributed as spaced apart data in accordance with a specified instruction”; and restoring said original positions of said idle/unassigned cells within said cell stream based upon said recorded original positions after transmission of said frame over a link (col. 7, line 56-26). Wolf does not expressly disclose that a wireless link is used; however, Examiner takes official notice that wireless transmission is very well known in the art. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to transmit the ATM stream over a wireless link.

36. Claims 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al (USPN 5,425,101) in view of Scarpa (USPN 5,444,743).

37. Regarding claim 34, Woo discloses a method for decoding interleaved and encoded data received over a wireless link comprising: detecting a predetermined synchronization pattern in said encoded data received over said wireless link (col. 4, lines 50-57); passing said data to a deinterleaver and decoder when said predetermined synchronization pattern has been detected (col. 6, line 32-col. 7, line 49); determining a number of bytes in error in said data (col. 6, line 32-col. 7, line 49). Woo does not expressly disclose declaring a synchronization mode when the number of bytes in error between successive synchronization patterns is less than a predetermined number. Scarpa teaches, in a communication system, declaring a synchronization mode when the number of bytes in error between successive synchronization patterns is less than a predetermined number (col. 1, line 57-col. 2, line 28) where it is implicit that this is done in order to ensure that synchronization is properly achieved. It would have been obvious to one of ordinary skill in the art at the time of the invention to declare a synchronization mode when the

number of bytes in error between successive synchronization patterns is less than a predetermined number in order to ensure that synchronization is properly achieved.

38. Regarding claim 35, referring to claim 34, Woo in view of Scarpa discloses that the step of detecting includes setting a pattern search window of a predetermined number of bytes (Scarpa: col. 1, line 57-col. 2, line 28).

39. Regarding claim 36, referring to claim 34, Woo in view of Scarpa discloses declaring an identification of said synchronization pattern when a predetermined number of bytes of data are detected as matching said predetermined synchronization pattern (Scarpa: col. 1, line 57-col. 2, line 28).

40. Regarding claim 37, referring to claim 36, Woo in view of Scarpa does not disclose that the predetermined number of bytes is two; however, Woo in view of Scarpa does disclose that there is a predetermined number of bytes (Scarpa: col. 1, line 57-col. 2, line 28). It is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1055); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Since Woo in view of Scarpa discloses that there is a predetermined number of bytes, any number of bytes, including two bytes, would have been obvious absent a showing of criticality by Applicant.

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41. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al (USPN 5,425,101).

42. Regarding claim 38, Woo suggests a method for decoding interleaved and encoded data transmitted and received over a wireless link comprising: deinterleaving said data and rearranging said data into a predetermined frame (col. 4, lines 50-57 and col. 9, lines 28-43); decoding said data according to a predetermined coding scheme (col. 4, lines 50-57 and col. 9, lines 28-43); detecting if any cells within a Header frame within said predetermined frame are uncorrectable (col. 4, lines 50-57 and col. 9, lines 28-43). Woo do not expressly disclose replacing detected uncorrectable cells with idle/unassigned cells; however, Examiner takes official notice that this is well known in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to drop a cell that cannot be corrected as is well known in the art.

Allowable Subject Matter

43. Claim 14 is allowed. The prior art does not disclose or fairly suggest overwriting the header bytes of each moved idle/unassigned cell with the recorded original positions of each corresponding moved idle/unassigned cell.

44. Claim 18 is allowed. The prior art does not disclose or fairly suggest recording a position of each said first flagged nibble encountered in each said predetermined number of ATM cells in control bytes contained in said header frame.

45. Claim 39 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not disclose or fairly suggest reading a plurality of

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header bytes within said Header frame and forming a table of sequence numbers based upon the read header bytes and reinserting idle/unassigned cells into the correct positions in the predetermined frame based upon the table of sequence numbers thereby restoring an order of cells occurring at a transmitting end of said wireless link.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (703)305-6970. The examiner can normally be reached on Mon.-Fri. 7:00-5:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703)308-6602. The fax phone number for the organization where this application or proceeding is assigned is (703)308-6743.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Daniel J. Ryman
Examiner
Art Unit 2665

DJR

Daniel J. Ryman



HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600